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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/066,603	02/06/2002	Kaoru Mori	100353-00099	5436

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EXAMINER	
AUDUONG, GENE NGHIA	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/08/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/066,603	MORI ET AL.	
	Examiner	Art Unit	
	Gene N Auduong	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is FINAL. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disp sition of Claims

4)☒ Claim(s) 1-15 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-15 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the applicant:

- Information Disclosure Statement (IDS), filed on February 6, 2002.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Bertin et al. (U.S. Pat. No. 5,946,545).

Regarding claim 1, Bertin et al. disclose a semiconductor memory device, comprising: a data buffer for inputting/outputting data from/to an exterior of the device (figure 6, col. 9, lines 1+); a plurality of DRAM cell array blocks (col. 9, lines 12+); an SRAM redundancy cell disposed peripheral portion of the plurality of DRAM cell array blocks (col. 4, lines 26+); a fuse circuit which stores an address of a defect memory cell in the DRAM cell array blocks (col. 6,

lines (col. 6, lines 45+); a comparison circuit which compares an input address with the address stored in the fuse circuit; and an I/O bus which couple the SRAM redundancy cell to the data buffer in response to an address match signal from the comparison circuit (col. 5, lines 39+; col. 6, lines 17+ and its description).

Regarding claims 2, 4, 6 and 15, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 1, Bertin et al. further include a sense amplifier line that is provided for each of the plurality of DRAM cell array blocks (figures 6-8, each of the memory cell chips in the stacks), wherein the SRAM redundancy cell is provided in part of an area generally allocated the sense amplifier line (figures 6-8).

Regarding claims 3, 5, 8, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 1, Bertin et al. further includes a sub-word decoder that is provided for each of the plurality of DRAM cell array blocks (figures 6-8, each word/decode driver for each chip in the stack), wherein the SRAM redundancy cell is provided in part of an area generally allocated to the sub-word decoder (col. 5, lines 39+, col. 8, lines 9+).

Regarding claim 7, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 1, Bertin et al. further comprising a column decoder (figure 8, bit decoder) that is provided for each of the plurality of DRAM cell array blocks (see figure 8), wherein the SRAM redundancy cell is situated in part of an area generally allocated to the column decoder (col. 5, lines 39+).

Regarding claims 9-11, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 1, wherein the SRAM redundancy cell which is situated around each of the plurality of DRAM cell array blocks has a memory capacity for

replacing a single defect location in the DRAM cell array blocks, wherein the SRAM redundancy cell is capable of replacing a defect memory cell located in any one of the plurality of DRAM cell array blocks, wherein the fuse circuit is set such that when two or more defect locations are present in one of the DRAM cell array blocks, at least one of the defect locations is replaced by the SRAM redundancy cell of another one of the DRAM cell array blocks (col. 5, lines 39+).

Regarding claim 12, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 1, wherein the comparison circuit compares a row address, a block address, and a column address of the input address with the address stored in the fuse circuit (col. 8, lines 39+ and its description).

Regarding claim 13, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 12, Bertin et al. further comprising: a word decoder which selectively activates a word line corresponding to the row address of the input address regardless of the comparison made by the comparison circuit; a column decoder which selectively activates a column line corresponding to the column address of the input address in response to an unmatched result found by the comparison circuit, and selectively activates a redundant column line corresponding to the SRAM redundancy cell in response to the address match found by the comparison circuit (col. 5, lines 39+, col. 8, lines 9+).

Regarding claim 14, Bertin et al. disclose the semiconductor memory device comprising all of the limitation as claimed in claim 13, wherein a number of bits of SRAM redundancy cells selected by the redundant column line is equal to a number of bits of data selected by the column line (col. 5, lines 39+).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Ferrant US2002/0001242.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Auduong whose telephone number is (703) 305-1343.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (703) 308-4910. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9318 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

GA
April 29, 2003

Gene N Auduong
Examiner
Art Unit 2818